The TAU 2014 Contest

Removing Pessimism during Timing Analysis

Sponsors:

Jin Hu
IBM Corp.
[Speaker]

Debjit Sinha
IBM Corp.

Igor Keller
Cadence

TAU 2014 Workshop – March 6th-7th, 2014
Past and Present Timing Contests

Goal of Coordinated Academic-Industry Contests
- Guided awareness of challenging projects at earlier academic stages
- Encourage novel parallelization techniques (including multi-threading)
- Facilitate infrastructure/benchmarks for future research

Develop Clever Methods for Solving Difficult Problems
- Gain insight from other perspectives and approaches
- Allow algorithm development through focused problem statement

Previous Contests

PATMOS'2011
Timing Analysis Contest

TAU 2013 contest: Variation aware timing analysis
Focused Problem Statement

Develop an algorithm to perform

**Common Path Pessimism Removal (CPPR)**

during timing analysis

*CPPR: the process of removing inherent but artificial pessimism from timing tests and paths*
Variability causes many sources of timing uncertainty

Difficult to **accurately** and **quickly** model for all variation sources

Create **lower** (early) and **upper** (late) delay bounds $[lb, ub]$

- Commonly found by **derating** original delay, e.g., $\pm 5\%$
- Any unknown, difficult-to-model effect can be accounted for

**Good news:** additional *pessimism* introduced (desirable for safe chip operation)

**Bad news:** additional *pessimism* introduced (unnecessary)

CPPR prevents over-optimization of design due to **false timing fails**
Sequential Timing Analysis

**Hold** Tests *(Same Cycle)*

\[
slack_{\text{HOLD}} = \text{at } (D) - \text{at } (CK) - t_{\text{HOLD}}
\]

- **pre-CPPR slack**
- **arrival time at D**
- **arrival time at CK**
- **hold time**

*Timing tests are checked against data pin D and clock pin CK of FF*

Details provided in contest_education.pdf

[data must be stable \( t_{\text{HOLD}} \) time after clock arrives]
Sequential Timing Analysis

Hold Tests *(Same Cycle)*

\[
\text{slack}_{\text{HOLD}} = \text{at}^E(D) - \text{at}^L(CK) - t_{\text{HOLD}}
\]

- **pre-CPPR slack**: early arrival time at D
- **late arrival time at CK**: hold time

Timing tests are checked against data pin D and clock pin CK of FF at opposite modes

*Data must be stable* \( t_{\text{HOLD}} \) *time after clock arrives*
Sequential Timing Analysis

**Hold** Tests *(Same Cycle)*

\[ slack_{HOLD} = at^E(D) - at^I(CK) - t_{HOLD} \]

- **pre-CPPR slack**
  - early arrival time at \( D \)
  - late arrival time at \( CK \)
  - hold time

[Data must be stable \( t_{HOLD} \) time after clock arrives]

Timing tests are checked against **data pin** \( D \) and **clock pin** \( CK \) of FF at opposite modes

Signal cannot be both early and late in common portion

\( \Rightarrow \) This is inherent but artificial pessimism
Common Path Pessimism Removal

**Hold** Tests (*Same Cycle*)

\[
\text{slack}_{\text{HOLD}} = \text{at}^E(D) - \text{at}^L(CK) - t_{\text{HOLD}}
\]

*post-CPPR slack*  
early arrival time at *D*  
late arrival time at *CK*  
hold time

[data must be stable \(t_{\text{HOLD}}\) time after clock arrives]

\[
+ [\text{at}^L(cp) - \text{at}^E(cp)]
\]

Apply [Hold CPPR credit]

Timing tests are checked against data pin *D* and clock pin *CK* of FF at opposite modes

IN \[\rightarrow\] Launching FF \(_1\) \[\rightarrow\] Capturing FF \(_2\) \[\rightarrow\] OUT

Signal cannot be both early and late in *common portion*  
\(\Rightarrow\) This is inherent but artificial pessimism
Common Path Pessimism Removal

**Hold** Tests (*Same Cycle*)

\[
\text{slack}_{\text{HOLD}} = \text{at}^E(D) - \text{at}^L(CK) - t_{\text{HOLD}}
\]

Post-CPPR slack \[\text{at}^E(D)\text{ early arrival at } D\]
\[\text{at}^L(CK)\text{ late arrival at } CK\]
\[t_{\text{HOLD}}\text{ hold time}\]

\[\text{Apply [Hold CPPR credit]}\]

**Setup** Tests (*Next Cycle with clock period* \(P\))

\[
\text{slack}_{\text{SETUP}} = \text{at}^E(CK) + P - \text{at}^L(D) - t_{\text{SETUP}}
\]

Post-CPPR slack \[\text{at}^E(CK)\text{ early arrival at } CK\]
\[P\text{ clock period}\]
\[\text{at}^L(D)\text{ late arrival at } D\]
\[t_{\text{SETUP}}\text{ setup time}\]

\[\text{Apply [Setup CPPR credit]}\]

\[\text{OL} = \text{CP} \cap \text{DP}\]

**Timing tests** are checked against **data pin** \(D\) and **clock pin** \(CK\) of FF at opposite modes

\[\text{data must be stable } t_{\text{HOLD}} \text{ time after clock arrives}\]

\[\text{data must be stable } t_{\text{SETUP}} \text{ time before clock arrives}\]

**Signal cannot be both early and late in common portion**

\[\Rightarrow \text{This is inherent but artificial pessimism}\]
Potential Impact of CPPR

**CPPR can only improve test slacks (never overly optimistic)**

*if done correctly*

Pre-CPPR slack ≈ -55
Post-CPPR slack ≈ +275

no post-CPPR slack worse than its pre-CPPR slack

pre-CPPR slack = post-CPPR slack
TAU 2014 Contest Motivation

**CPPR Challenges**
- Analysis is path-based: can have **exponential runtime**
  - CPPR can be overly optimistic if not enough paths are considered
- Existing literature and research is **limited**

**Contest / Topic Scope**
- Timeline spans roughly **2.5 months** *not accounting for holidays*
- Only Hold + Setup tests considered
- No latches (flush segments) considered
- Limited design topologies, e.g., clock tree reconvergence
- Limited to deterministic timing (no statistical)

**Lessons Learned from Previous Contests**
- Simplify input / output processing
  - focus on algorithm development and performance optimizations
- Provide adequate documentation
  - assumes **no** prior knowledge of timing analysis or CPPR
TAU 2014 Contest Guidelines

Pre-processing

- TAU 2013 Benchmarks
- Design Library
- Delay Converter
  Phase 1
- Industrial Tool
  Phases 2 and 3

Provided to Contestants

- Detailed Documentation
- Delay File
  Topology, tests, etc.
- Timing File
  Assertions, etc.

Evaluation

- Path-based CPPR Output
- Golden Result*

*Industrial tool
Inputs: Delay File

- Specifies **primary inputs** and **outputs**
- Provides **early** and **late** propagation delay for every source-to-sink timing arc
- Provides **setup** and **hold** times for every data-to-clock timing test

Details provided in contest_file_formats.pdf
**Inputs: Timing File**

- Provides **early** and **late arrival times** for each **primary input**
- Provides **clock period** for the **clock source**

---

**Diagram Description**

- **FF**
  - Setup
  - Hold
  - **CK**

- **OR2**
  - **A**
  - **B**
  - **Y**

- **B**
  - **A**
  - **Y**

- **Primary Input**
  - **IN1**
  - **IN2**

- **CLOCK**
  - **B1**
  - **B2**
  - **B3**
  - **B4**

- **FF1**
  - **FF2**
  - **FF3**

- **Timing Arc**
  - **Timing Test**

- **Primary Input**
  - **at IN1 0e+0 1e-11**
  - **early at**
  - **late at**

- **clock CLOCK 1.2e-10**
  - **clock pin**
  - **clock period**

*Details provided in contest_file_formats.pdf*
Output File

- Requires pre-CPPR and post-CPPR slacks for each test and path
- Controllable options: `<testType>` -numTests <int> -numPaths <int>
  [setup/hold/both] [number of tests] [number of paths per test]

Details provided in contest_file_formats.pdf
contest_rules.pdf

Controllable options:
- `setup -3e-11 -1e-11 1`
- `test type` -numPaths
- `pre-CPPR` test slack
- `post-CPPR` test slack
- `path length`
- `-1.5e-11 -1e-11 10`
- `pre-CPPR` path slack
- `post-CPPR` path slack

Pin-to-pin data path from: data pin of test to: primary input
### Benchmarks

#### Phase 1
- **[6-42 Tests]**
- Based on TAU 2013 v1.0 benchmarks (sequential circuits)

<table>
<thead>
<tr>
<th>Design</th>
<th>Number of:</th>
<th>Tests</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PIs</td>
<td>POs</td>
</tr>
<tr>
<td>s27</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>s344</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>s349</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>s386</td>
<td>9</td>
<td>7</td>
</tr>
<tr>
<td>s100</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>s510</td>
<td>21</td>
<td>7</td>
</tr>
<tr>
<td>s526</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>s1196</td>
<td>16</td>
<td>14</td>
</tr>
<tr>
<td>s1494</td>
<td>10</td>
<td>19</td>
</tr>
</tbody>
</table>

#### Phase 2
- **[380-50.1K Tests]**
- Based on TAU 2013 v2.0 benchmarks (openCore)

<table>
<thead>
<tr>
<th>Design</th>
<th>Number of:</th>
<th>Tests</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PIs</td>
<td>POs</td>
</tr>
<tr>
<td>systemcdes</td>
<td>132</td>
<td>65</td>
</tr>
<tr>
<td>wb_dma</td>
<td>217</td>
<td>215</td>
</tr>
<tr>
<td>tv80</td>
<td>14</td>
<td>32</td>
</tr>
<tr>
<td>systemcaes</td>
<td>260</td>
<td>129</td>
</tr>
<tr>
<td>mem_ctrl</td>
<td>115</td>
<td>152</td>
</tr>
<tr>
<td>ac97_ctrl</td>
<td>84</td>
<td>48</td>
</tr>
<tr>
<td>usb_func</td>
<td>128</td>
<td>121</td>
</tr>
<tr>
<td>pci_bridge32</td>
<td>162</td>
<td>207</td>
</tr>
<tr>
<td>aes_core</td>
<td>260</td>
<td>129</td>
</tr>
<tr>
<td>des_perf</td>
<td>235</td>
<td>64</td>
</tr>
<tr>
<td>vga_lcd</td>
<td>89</td>
<td>109</td>
</tr>
</tbody>
</table>

#### Phase 3
- (Evaluation)
- **[8.2K to 109.6K Tests]**

<table>
<thead>
<tr>
<th>Design</th>
<th>Number of:</th>
<th>Tests</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PIs</td>
<td>POs</td>
</tr>
<tr>
<td>Combo2</td>
<td>170</td>
<td>218</td>
</tr>
<tr>
<td>Combo3</td>
<td>353</td>
<td>215</td>
</tr>
<tr>
<td>Combo4</td>
<td>260</td>
<td>109</td>
</tr>
<tr>
<td>Combo5</td>
<td>432</td>
<td>164</td>
</tr>
<tr>
<td>Combo6</td>
<td>486</td>
<td>174</td>
</tr>
<tr>
<td>Combo7</td>
<td>459</td>
<td>148</td>
</tr>
</tbody>
</table>

- Added more complex (randomized) clock tree
  - \( \text{BRANCH}(\text{CLOCK, initial \text{FF}}) \)
  - For each remaining \text{FF}
    - \( \text{BRANCH}(L,\text{FF}) \)
    - \( \text{BRANCH}(\text{src,sink}) : \text{create buffer chain from src to sink} \)
Evaluation Metrics

- **Accuracy (Compared to “Golden” Results)**
  - Test \( t \) Slack Accuracy \( A(t) \)
    - Pre-CPPR test slack
    - Post-CPPR test slack
  - Path \( p \) Slack Accuracy \( A(p) \)
    - Pre-CPPR path slack
    - Post-CPPR path slack
    - Correctness of path

- **Slack Accuracy (Difference)**
  
<table>
<thead>
<tr>
<th>Interval</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>([0, 1])</td>
<td>100</td>
</tr>
<tr>
<td>((1, 3])</td>
<td>80</td>
</tr>
<tr>
<td>((3, 5])</td>
<td>50</td>
</tr>
<tr>
<td>((5, \infty])</td>
<td>0</td>
</tr>
</tbody>
</table>

- **Runtime Factor (Relative)**
  \[
  RF(D) = \frac{\text{runtime}(D)}{\text{Average of all contestants}}
  \]

- **Composite Testcase Score**
  \[
  \text{score}(D) = A(D) \times (0.5 + 0.5 \times RF(D))
  \]

- **Overall Contestant Score**
  \[
  \text{Average of score}(D) \text{ for all designs}
  \]

- **Memory usage not considered**

---

\( T: \) set of all tests in \( D \)

\( P: \) set of all paths in \( D \)

---

\( T: \) set of all tests in \( D \)

\( P: \) set of all paths in \( D \)
**TAU 2014 Contestants**

<table>
<thead>
<tr>
<th>University</th>
<th>Country</th>
<th>Team Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>National Chiao Tung University</td>
<td>Taiwan</td>
<td>iTimerC</td>
</tr>
<tr>
<td>University of Thessaly</td>
<td>Greece</td>
<td>The TimeKeepers</td>
</tr>
<tr>
<td>National Tsing Hua University</td>
<td>Taiwan</td>
<td>TTT</td>
</tr>
<tr>
<td>India Institute of Technology, Madras</td>
<td>India</td>
<td>ElecEnthus</td>
</tr>
<tr>
<td>University of Illinois at Urbana-Champaign</td>
<td>USA</td>
<td>UI-Timer</td>
</tr>
<tr>
<td>India Institute of Technology, Madras</td>
<td>India</td>
<td>LightSpeed</td>
</tr>
<tr>
<td>Missouri University of Science and Technology</td>
<td>USA</td>
<td>MST_CAD</td>
</tr>
<tr>
<td>Peking University</td>
<td>China</td>
<td>PKU-HappyTimer</td>
</tr>
</tbody>
</table>
Contestant Performance

Overall quality of submitted binaries was superb

One testcase comprised of \(<\text{benchmark, testType, -numTests, -numPaths}> \rightarrow 24 \text{ total}\)

\[\text{For each Combo benchmark, used 4 settings: } \{\text{-setup, -hold}\} \times \{\text{-numTests N, -numPaths 1, -numTests n, -numPaths m}\}\]

Ex: Combo7 -setup -numTests 35000 -numPaths 1

\[\rightarrow 5 \text{ of 7 final submissions had } \text{no crashes}; \text{ 1 of 7 crashed on only 5 testcases}\]

\[\rightarrow 6 \text{ of 7 final submissions had full accuracy on 12 designs}\]

Evaluation Machine: 8X Intel(R) Xeon CPU E7-8837 @2.67GHz

\[\rightarrow 6 \text{ of 7 final submissions used 8 threads [maximum allowed]; }\]

\[1 \text{ of 7 final submissions used 2 threads}\]

---

<table>
<thead>
<tr>
<th>Team</th>
<th>(C_1)</th>
<th>(C_2)</th>
<th>(C_3)</th>
<th>(C_4)</th>
<th>(C_5)</th>
<th>(C_6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Runtime (hours)</td>
<td>6.27</td>
<td>4.27</td>
<td>1.44</td>
<td>7.8</td>
<td>4.96</td>
<td>2.42</td>
</tr>
</tbody>
</table>

*Final evaluation is design-specific, not based on total runtime or overall averages*
Acknowledgments

⇒ Jobin Kavalam, Nitin Chandrachoodan [IITimer from TAU 2013]
  Provided timer source code, helped with initial input file conversions

⇒ Debjit Sinha, Igor Keller, Chirayu Amin [TAU 2014 Committee]

Special Thanks to
the TAU 2014 Contestants

This contest would not have been successful
without your hard work and dedication
Winners
TAU 2014 Timing Contest
Removing Common Path Pessimism

Third Place Award
Presented to

Yu-Ming Yang, Yu-Wei Chang and Iris Hui-Ru Jiang

National Chiao Tung University, Taiwan

For
iTimerC

Chirayu Amin
General Chair

Igor Keller
Technical Chair

Jin Hu
Contest Chair
TAU 2014 Timing Contest
Removing Common Path Pessimism

Honorable Mention
Presented to
Christos Kalonakis, Charalampos Antoniadis, Panagiotis Giannakou, Dimos Dioudis, George Pinitas and George Stamoulis
University of Thessaly, Greece
For
The TimeKeepers

Chirayu Amin
General Chair
Igor Keller
Technical Chair
Jin Hu
 Contest Chair
TAU 2014 Timing Contest
Removing Common Path Pessimism

Second Place Award
Presented to

M S Santosh Kumar and Sireesh N

IIT Madras, India

For
LightSpeed

Chirayu Amin
General Chair

Igor Keller
Technical Chair

Jin Hu
Contest Chair
TAU 2014 Timing Contest
Removing Common Path Pessimism

First Place Award
Presented to

Tsung-Wei Huang, Pei-Ci Wu and Martin D. F. Wong

University of Illinois at Urbana-Champaign, USA

For
UI-Timer

Chirayu Amin
General Chair

Igor Keller
Technical Chair

Jin Hu
Contest Chair
Backup
# Contest Timeline

<table>
<thead>
<tr>
<th>Date</th>
<th>Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>10/13/2013</td>
<td>Contest release date [<a href="https://sites.google.com/site/taucontest2014%5C">https://sites.google.com/site/taucontest2014\</a>] &lt;br&gt;• Timing analysis and CPPR tutorial [contest_education.pdf]  &lt;br&gt;• Contest overview and guidelines [contest_rules.pdf]  &lt;br&gt;• Contest input and output specifications [contest_file_formats.pdf]  &lt;br&gt;• Source code from the winners of TAU 2013 Contest (IITimer)</td>
</tr>
<tr>
<td>11/22/2013 – 12/02/2013 – 01/06/2014</td>
<td>End of contest registration  &lt;br&gt;• Phase 1 Benchmark Set [9 testcases]  &lt;br&gt;• Phase 2 Benchmark Set [6 testcases]</td>
</tr>
<tr>
<td>01/15/2014</td>
<td>Alpha binary submission</td>
</tr>
<tr>
<td>02/01/2014 [~2.5 months]</td>
<td>Final binary + short report submission</td>
</tr>
<tr>
<td>03/07/2014</td>
<td>Winners announced (today!)</td>
</tr>
</tbody>
</table>