TAU Workshop 2014

Increasing the Accuracy of Interconnect Derates: A Path Based Method

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Overview

- Sources of interconnect variation
- Impact of interconnect variation
- Standard interconnect variation margining methodologies
- Proposed interconnect variation margining methodology
- Future work and conclusions
Sources of Interconnect Variation

- Lithography
  - Optical Proximity Correction
  - Position in the optical field
  - Lens aberrations
  - Mask imperfections
- Planarization
  - Chemical Mechanical Planarization
- Deposition/Etch
- Environmental factors
  - Misalignment between lithographic steps
  - Different equipment used on adjacent metal layers
  - Temperature & pressure
Impact of Interconnect Variation

- Comparison of interconnect delays in timing environments differentiated only by parasitic corner, in this case Best/Worst
- Note that SI analysis was disabled
Impact of Interconnect Variation
Impact of Interconnect Variation
Standard Margining Methodologies

- Statistical STA
- Associated problems:
  i. Considerable resource requirements
  ii. Complexity
  iii. Availability of statistical models
  iv. Known limitations e.g. error associated with MIN/MAX operations
  v. Additional licenses
Standard Margining Methodologies

- Using vendor provided timing margin recommendations
- These vary from vendor to vendor but are likely to look similar to the following:

<table>
<thead>
<tr>
<th>Signoff Timing Corner</th>
<th>BC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signoff Parasitic Corners</td>
<td>Best</td>
</tr>
<tr>
<td>Check Types</td>
<td>Hold</td>
</tr>
<tr>
<td>Max Transition</td>
<td>0.5ns</td>
</tr>
<tr>
<td>Capture Path OCV</td>
<td>+10%</td>
</tr>
<tr>
<td>Extra Margin</td>
<td>100ps</td>
</tr>
</tbody>
</table>
Standard Margining Methodologies

- Applying the example timing recommendations

All interconnects on launch/data paths assume *Best* parasitics.

All interconnects on capture path assume delay as per *Best* parasitics offset by +10%.

Hold Check
Standard Margining Methodology

-associated problems:

i. Assumed that using *Best* parasitics on the launch and data paths is conservative

ii. Assumed that using *Best* parasitics on the capture path, with the resultant delays offset by 10%, is conservative

iii. Impact of interconnect variation on directly connected cells is not considered

iv. Susceptibility of individual paths to interconnect variation is not considered

v. Number of paths with little or no slack is not considered
Proposed Margining Methodology

Consider the ways in which varying interconnect RC affects non-SI path delay:

i. It affects base interconnect delay $(D_{\text{NET}})$

ii. It affects propagation delay through the directly connected upstream cell $(D_{\text{CELL-UP}})$

iii. It affects delay through directly connected downstream cells $(D_{\text{CELL-DOWN}})$
Proposed Margining Methodology

- SI analysis is disabled
- Initially, STA is run as before using vendor recommended timing margins
- The proposed methodology is then applied to paths with little or no slack on each signoff corner
Proposed Margining Methodology

Assume for illustration purposes that...

i. A single timing corner, e.g. \texttt{ss\_wcv\_125}, is being used

ii. A single fixed set of constraints are being used

iii. Two parasitic corners, \texttt{Best/Worst}, are being used
Proposed Margining Methodology

- STA is rerun on each corner with no interconnect derates applied
- Instead of derates, the most pessimistic parasitic corner is used for each interconnect
- Most pessimistic parasitic corner determined using:
  - $(D_{NET} + D_{CELL-UP} + D_{CELL-DOWN})$
- Let…

<table>
<thead>
<tr>
<th>Alias</th>
<th>Definition</th>
<th>Parasitic Corner</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{ALL-BEST}$</td>
<td>$D_{NET} + D_{CELL-UP} + D_{CELL-DOWN}$</td>
<td>Best</td>
</tr>
<tr>
<td>$D_{ALL-WORST}$</td>
<td>$D_{NET} + D_{CELL-UP} + D_{CELL-DOWN}$</td>
<td>Worst</td>
</tr>
</tbody>
</table>
Proposed Margining Methodology

- Assume a hold check on the **Best** parasitic corner
- All launch and data path interconnects should be modelled as early
- If $D_{\text{ALL-WORST}} < D_{\text{ALL-BEST}}$ on any interconnect along either the launch or data paths, the slack is adjusted by $(D_{\text{ALL-BEST}} - D_{\text{ALL-WORST}})$ in each instance
Proposed Margining Methodology

- Similarly, all capture path interconnects should be modelled as late.
- If $D_{ALL-WORST} > D_{ALL-BEST}$ on any interconnect along the capture path, the slack is adjusted by $(D_{ALL-WORST} - D_{ALL-BEST})$ in each instance.

Hold Check

All capture path interconnects should be as late as possible.
Proposed Margining Methodology

- How is $D_{\text{NET}}$ measured?
  - Min/max rise/fall $D_{\text{NET}}$ is captured on each parasitic corner during initial STA
Proposed Margining Methodology

How are $D_{\text{CELL-UP}}/D_{\text{CELL-DOWN}}$ measured?

- In the previous example, would like to have annotated each individual net with *Worst* parasitics in turn
- Not currently supported by STA tools
- Workaround is to determine the relative change in $D_{\text{CELL-UP}}/D_{\text{CELL-DOWN}}$ across parasitic corners using lumped RC information captured during initial STA

- For example:
  - $D_{\text{CELL-UP}}$ using lumped *Best* = 300 ps
  - $D_{\text{CELL-UP}}$ using lumped *Worst* = 330 ps
  - $D_{\text{CELL-UP}}$ using *Best* = 200 ps
  - $D_{\text{CELL-UP}}$ using *Worst* assumed to be 220 ps
Proposed Margining Methodology

- A real example of the differences in resultant slack between the proposed methodology and using vendor provided timing margins on 28nm and 40nm CMOS processes
- The 100 most critical hold and setup paths were considered
Proposed Margining Methodology
Proposed Margining Methodology
Proposed Margining Methodology
Proposed Margining Methodology
Future Work

- Include additional designs
- Include additional 65nm CMOS process
- Compare slacks using various methods to slacks from using Monte Carlo SPICE simulations with statistical interconnect models
- Expand methodology to account for the effects of SI
- Account for the susceptibility paths to interconnect variation
- Account for the number of paths with little or no slack
Conclusions

- Standard interconnect variation margining methodologies are complex, or guesses
- The proposed methodology represents a reasonable trade-off between accuracy and complexity
- How path delays are affected by interconnect variation is modelled
- A more accurate and robust analysis with respect to using vendor recommended timing margins
Acknowledgements

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